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In re Application of

Chang Ho DO

Serial No. NOT YET ASSIGNED

Filed: May 21, 1999

For: A MULTI-BANK TESTING APPARATUS FOR A SYNCHRONOUS DRAM

TRANSMITTAL LETTERAssistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Submitted herewith for filing in the U.S. Patent and Trademark Office is the following:

- (1) Transmittal Letter
- (2) PTO Form-1082
- (3) 28 page Application consisting of:
 - 14 pages of Textual Specification
 - 5 pages of 8 Claims
 - 1 Abstract of the Disclosure
 - 8 sheets of drawings
- (4) Executed Inventor's Declaration
- (5) Assignment with recordation cover sheet
- (6) Request for Priority
- (7) Priority Document No. 1998 18885
- (8) Information Disclosure Statement with 2 references
- (9) PTO Form 1449
- (10) Check No. 11389 \$760.00 for the Government Filing Fee
- (11) Check No. 11390 \$ 40.00 for the Assignment recordation

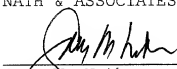
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FORM PTO-1082

TRANSMITTAL FOR NEW U.S. PATENT APPLICATION

Assistant Commissioner for
Patents and Trademarks
Washington, D.C. 20231

Re: New U.S. Patent Application

For: **A MULTI-BANK TESTING APPARATUS FOR A
SYNCHRONOUS DRAM**

Inventor(s): Chang Ho DO

Attorney Docket: 23900

Sir:

Attached hereto is the application identified above, includ-
ing:

- 28 Pages Application Consisting of:
14 Pages of Textual Specification
5 Pages of 8 Claims
1 Abstract of the Disclosure
8 Sheets of drawings.
x Executed Inventor's Declaration
x Assignment and cover sheet

The Government filing fee* is calculated as follows:

Total Claims	<u>8</u> - 20 = <u>0</u>	x \$18.00 =	<u>\$0.00</u>
Independent Claims	<u>1</u> - 3 = <u>0</u>	x \$78.00 =	<u>\$0.00</u>
Base Fee			<u>\$760.00</u>
Multiple Dependent Claim Fee (\$250.00)			<u>\$ 0.00</u>
Subtotal			<u>\$760.00</u>

TOTAL FILING FEE*

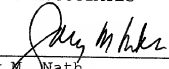
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- *Reduced by one-half, as applicant(s) is/are a "small entity".
A Declaration Claiming Small Entity Status:
- will be filed at a later date.
- is submitted herewith.
- ☒ Foreign priority is claimed under 35 U.S.C. § 119 from Korean Patent Application(s) No. 98-18885 dated May 25, 1998.
- Priority document(s) will be submitted at a later date.
- ☒ Priority document(s) is/are submitted herewith.
- Executed Declaration(s) will be submitted at a later date pursuant to 37 CFR § 1.41 and § 1.53, with an appropriate surcharge under 37 CFR § 1.16(e).
- ☒ Formal drawing(s) is/are attached.
- Formal drawing(s) will be submitted at a later date.
- ☒ Assignment document(s) is/are submitted herewith; the recordation fee of \$40.00 per document is enclosed herewith.
- A Verified Translation will be submitted at a later date.
- No payment is enclosed at this time. Full payment will be made when the executed Declaration is submitted.
- ☒ Submitted herewith is a check in the amount of \$760.00. The Commissioner is hereby authorized to charge any deficiency or credit any excess to Deposit Account No. 14-0112.

Respectfully submitted,

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(202)-775-8383

GMM/ph (1082)

A MULTI-BANK TESTING APPARATUS FOR A SYNCHRONOUS DRAM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an apparatus for testing a synchronous dynamic random access memory (DRAM) which is a semiconductor memory, and more particularly to a multi-bank testing apparatus for a synchronous DRAM, which allows all banks of the synchronous DRAM to simultaneously carry out their write and read operations in a test mode, thereby being capable of testing the entire bank in order to reduce the test time being likely to increase in accordance with an increased memory integration degree.

2. Description of the Related Art

Generally, a synchronous DRAM includes a plurality of row address strobe (RAS) generating circuits corresponding respectively to banks of the synchronous DRAM. Each of the RAS-generating circuits is enabled in response to a bank selection address signal adapted to select a bank associated with the RAS-generating circuit, thereby establishing row paths for the selected bank. The synchronous DRAM also includes a plurality of column address strobe (CAS) generating circuits corresponding respectively to the banks of the synchronous DRAM. Each of the CAS-generating circuits is enabled in response to a bank selection address signal adapted to select a bank associated with the CAS-generating circuit, thereby establishing column paths for the selected bank.

The above operations of the row and column address strobe generating circuits will now be described in conjunction with Figs. 1 and 2.

When a row active command is inputted to a synchronous DRAM in a normal operation mode, it enables a row address strobe signal which is a command signal for enabling RAS-generating circuits. This row address strobe signal is applied to RAS-generating circuits (denoted by "rasgen" in Fig. 1) 3 of all banks in the synchronous DRAM. Simultaneously, a bank selection address signal, which selects one of the banks, is applied to RAS-generating circuits 3 of all banks. Only the RAS-generating circuit 3 of the bank selected by the received bank selection address signal is enabled, based on the received row address strobe signal, to output a row address strobe enable signal, thereby establishing row paths for the selected bank. As a result, a word line associated with the enabled bank is enabled.

On the other hand, when a column active command is inputted to the synchronous DRAM, it enables a column address strobe signal which is a command signal for enabling CAS-generating circuits. This column address strobe signal is applied to CAS-generating circuits (denoted by "casgen" in Fig. 1) 4 of all banks in the synchronous DRAM. Simultaneously, a bank selection address signal, which selects one of the banks, is applied to CAS-generating circuits 4 of all banks. Only the CAS-generating circuit 4 of the bank selected by the received bank selection address signal is enabled, based on the received column address strobe signal, to output a column address strobe enable signal, thereby establishing column paths for the selected bank. As a result, a signal Yi, serving to couple each of bit lines to an associated one of local data bus lines LDB in an enable state thereof, is enabled. Accordingly, it is possible to carry out data read and write operations for the selected bank.

The above-mentioned data paths will be described in more detail, in conjunction with Fig. 1.

First, a description will be made in regard to the write paths.

Buffered data from each of data input buffers 11 is sent to an associated one of global write data bus lines GWDB, and is then sent
5 to an associated one of local data bus lines LDB in accordance with an operation of an associated one of write drivers WD.

10 In this state, when the signal Yi, serving to couple each local data bus line LDB to an associated one of bit lines in an enable state thereof, is enabled, the data from each local data bus line LDB is applied to an associated one of cells 1 via an associated bit line, so that it is stored in the associated cell 1.

Next, a description will be made in regard to the read paths.

15 When data from each cell 1 in a selected bank is sent to an associated bit line in accordance with a row active command, the signal Yi is enabled in response to the row active command, thereby causing the data from the bit line to be transmitted to an associated
20 local data bus line LDB. The data from the local data bus line LDB is then sent to an associated input/output sense amplifier 5 which, in turn, amplifies the data. The amplified data is subsequently transmitted to an associated global read data bus line GRDB, so that it is output through an associated data output buffer 12.

25 As mentioned above, a synchronous DRAM, which consists of N banks, conducts row and column activating operations for only one particular bank selected by a bank selection address BA every time the bank selection address BA is generated. For this reason, the testing
30 operation for such a synchronous DRAM is carried out for one bank.

In order to test the entire bank of the synchronous DRAM, it is necessary to conduct the testing operation by N times corresponding to the number of banks in the synchronous DRAM. This results in a lengthened test time.

5

SUMMARY OF THE INVENTION

Therefore, the present invention has been made in view of the above-mentioned problems involved in conventional techniques, and an object of the invention is to provide a multi-bank testing apparatus for a synchronous DRAM which allows all banks of the synchronous DRAM to simultaneously carry out their write and read operations in a test mode, thereby being capable of testing the entire bank in order to reduce the test time being likely to increase in accordance with an increased memory integration degree.

In accordance with the present invention, this object is accomplished by providing a multi-bank testing apparatus for a synchronous DRAM consisting of a plurality of banks, comprising: a row address strobe generating unit for enabling a word line to transmit data from cells to bit line sense amplifiers in each bank of said synchronous DRAM; a column address strobe generating unit for generating a signal adapted to enable transistors respectively adapted to couple bit lines carrying data, amplified by said bit line sense amplifiers, to local data bus lines; input/output sense amplifiers for amplifying data on said local data bus lines, respectively; a transmission gate unit for controlling transmission of data from said input/output sense amplifiers to global read data bus lines; and an input/output comparing unit for compressing data from said input/output sense amplifiers prior to said transmission thereof to said global read data bus lines.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and aspects of the invention will become apparent
5 from the following description of embodiments with reference to the
accompanying drawings in which:

Fig. 1 is a block diagram illustrating a configuration of a
general synchronous DRAM;

10 Fig. 2 is a block diagram illustrating output paths for
input/output sense amplifiers shown in Fig. 1;

Figs. 3a and 3b are diagrams illustrating a configuration of
a RAS-generating circuit unit included in a multi-bank testing
apparatus according to the present invention;

15 Figs. 4a and 4b are diagrams illustrating a configuration of
a CAS-generating circuit unit included in the multi-bank testing
apparatus according to the present invention;

Fig. 5 is a block diagram illustrating output paths for
input/output sense amplifiers in accordance with an embodiment of
the present invention;

20 Fig. 6 is a block diagram illustrating output paths for
input/output sense amplifiers in accordance with another embodiment
of the present invention;

Fig. 7 is a circuit diagram illustrating a configuration of a
transmission gate unit included in the multi-bank testing apparatus
25 according to the present invention; and

Fig. 8 is a circuit diagram illustrating a configuration of an
input/output comparing unit included in the multi-bank testing
apparatus according to the present invention.

30

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Figs. 3a to 8, circuits included in an apparatus for testing banks of a synchronous DRAM in accordance with the present invention are illustrated, respectively.

5 The testing apparatus of the present invention includes a RAS-generating unit 30 (Fig. 3a) for enabling a word line to transmit data from cells to bit line sense amplifiers 20 in each bank of a synchronous DRAM, a CAS-generating unit 40 (Fig. 4a) for generating a signal adapted to enable transistors respectively adapted to couple
10 bit lines carrying data, amplified by the bit line sense amplifiers 20, to local data bus lines LDB, and input/output sense amplifiers 50 for amplifying data on the local data bus lines LDB, respectively.

The testing apparatus also includes a transmission gate unit 60 for controlling transmission of data from the input/output sense
15 amplifiers 50 to global read data bus lines GRDB. The testing apparatus further includes an input/output comparing unit 70 for compressing data from the input/output sense amplifiers 50 prior to the transmission thereof to the global read data bus lines GRDB.

20 As shown in Fig. 3b, the RAS-generating unit 30 includes a PMOS transistor PM31 and an NMOS transistor NM31 connected in series to each other. A row address strobe signal is commonly applied to the gates of the PMOS transistor PM31 and the NMOS transistor NM31. A timing controller 31 is coupled to a node between the PMOS transistor
25 PM31 and the NMOS transistor NM31. The timing controller 31 serves to control the period of time for which an output from the RAS-generating unit 30, namely, a row address strobe enable signal rasatv, is in an enable state. A plurality of NMOS transistors NM32a to NM32z, which are coupled in series together, is connected in series to the
30 NMOS transistor NM 31. Each of the NMOS transistors NM32a to NM32z receives an associated one of bank selection address signals BAA to

BAZ at its gate. Another NMOS transistor NM30 is coupled to a node between the NMOS transistor NM31 and the NMOS transistor NM32a in a parallel fashion. The NMOS transistor NM30 receives, at its gate, a test signal for all banks (hereinafter, referred to as a "all-bank test signal"), tm_abwr . The all-bank test signal tm_abwr is enabled when write and read operations are to be conducted for all banks.

Referring to Fig. 4b, a detailed configuration of the CAS-generating unit 40 is illustrated. As shown in Fig. 4b, the CAS-generating unit 40 includes a PMOS transistor PM41 and an NMOS transistor NM41 connected in series to each other. A row address strobe signal is commonly applied to the gates of the PMOS transistor PM41 and the NMOS transistor NM41. A timing controller 41 is coupled to a node between the PMOS transistor PM41 and the NMOS transistor NM41. The timing controller 41 serves to control the period of time for which an output from the CAS-generating unit 40, namely a row address strobe enable signal $casatv$, is in an enable state. A plurality of NMOS transistors NM42a to NM42z, which are coupled in series together, is connected in series to the NMOS transistor NM41. Each of the NMOS transistors NM42a to NM42z receives an associated one of bank selection address signals BAa to BAZ at its gate. Another NMOS transistor NM40 is coupled in parallel to a node between the NMOS transistor NM41 and NMOS transistor NM42a. The NMOS transistor NM40 receives, at its gate, the all-bank test signal tm_abwr enabled when write and read operations are to be conducted for all banks.

The transmission gate unit 60 includes a plurality of first transmission gates 61 and a pair of second transmission gates 62, as shown in Figs. 5 and 6. Each first transmission gate 61 is arranged

between the output of an associated input/output sense amplifier 50 and an associated global read data bus line GRDB or bar-capped GRDB.

In a test mode, the first transmission gate 61 is closed, thereby preventing data from the associated input/output sense amplifier 50 from being transmitted to the associated global read data bus line GRDB or bar-capped GRDB. On the other hand, each second transmission gate 62 is arranged between the output of the input/output comparing unit 70 and an associated input/output global read data bus line GRDB or bar-capped GRDB. The second transmission gate 62 is opened in the test mode, thereby allowing the output from the input/output comparing unit 70 to be transmitted to the associated global read data bus line GRDB or bar-capped GRDB.

Referring to Fig. 7, a detailed configuration of each first transmission gate 61 and each second transmission gate 62 included in the transmission gate unit 60 is illustrated. As shown in Fig. 7, the first transmission gate 61 includes a PMOS transistor PM61 and an NMOS transistor NM61 coupled in parallel between an associated one of the input/output sense amplifiers 50 and one of two global read data bus lines GRDB and bar-capped GRDB respectively associated with input and input-bar signals from the input/output sense amplifier 50, that is, the global read data bus line GRDB. At its gate, the PMOS transistor PM61 receives the all-bank test signal tm_abwr whereas the NMOS transistor NM61 receives, at its gate, a signal inverted from the all-bank test signal tm_abwr via an inverter In60. The first transmission gate 61 also includes another PMOS transistor PM62 and another NMOS transistor NM62 coupled in parallel between the associated input/output sense amplifier 50 and the other associated global read data bus line, bar-capped GRDB. At its gate, the PMOS transistor PM62 receives the all-bank test signal tm_abwr whereas the NMOS transistor NM62 receives, at its gate, the signal

inverted from the all-bank test signal tm_abwr via the inverter In60.

On the other hand, the second transmission gate 62 includes a PMOS transistor PM63 and an NMOS transistor NM63 coupled in parallel between the input/output comparing unit 70 and the global read data bus line GRDB. The PMOS transistor PM63 receives, at its gate, the signal inverted from the all-bank test signal tm_abwr via the inverter In60 whereas the NMOS transistor NM63 receives, at its gate, the all-bank test signal tm_abwr. The second transmission gate 62 further includes another PMOS transistor PM64 and another NMOS transistor NM64 coupled in parallel between the input/output comparing unit 70 and the other global read data bus line, bar-capped GRDB. The PMOS transistor PM64 receives, at its gate, the signal inverted from the all-bank test signal tm_abwr via the inverter In60 whereas the NMOS transistor NM64 receives, at its gate, the all-bank test signal tm_abwr.

Fig. 8 illustrates a detailed configuration of the input/output comparing unit 70. As shown in Fig. 8, the input/output comparing unit 70 includes PMOS transistors PM71 and PM 76, and NMOS transistors NM71 and NM76. These PMOS and NMOS transistors PM71, PM76, NM71, and NM76 are coupled together in parallel and receive, at respective gates thereof, a signal inverted from the all-bank test signal tm_abwr via an inverter In70. A plurality of PMOS transistors PM72 to PM75 is coupled in parallel between the PMOS transistor PM71 and the NMOS transistor NM71. The PMOS transistors PM 72 to PM75 receive, at respective gates thereof, input signals IO<0:3> which are output from associated input/output sense amplifiers 50, respectively. An NMOS transistor NM72 is connected to the NMOS transistor NM71 in such a fashion that they have a common source. A plurality of PMOS transistors PM77 to PM80 is coupled in parallel between the PMOS transistor PM76 and NMOS transistor NM73. The PMOS transistors PM

77 to PM80 receive, at respective gates thereof, input-bar signals, bar-capped IO<0:3>, which are output from the associated input/output sense amplifiers 50, respectively. An NMOS transistor NM74 is connected to the NMOS transistor NM73 in such a fashion that they have a common source. The input/output comparing unit 70 also includes NAND gates NA71, NA72, and NA73. The NAND gate 71 receives output and output-bar signals from the associated input/output sense amplifiers 50. The NAND gate NA72 receives an output from the NAND gate NA71 along with the all-bank test signal tm_abwr. The NAND gate NA73 receives an output from the NAND gate NA72 via inverters In71 to In74 at one input thereof. The output from the NAND gate NA72 is also applied to the other input of the NAND gate NA73 via the inverters In71 to In74 and then via inverters In75 to In79. The output from the NAND gate NA73 is coupled to the gates of the NMOS transistors NM72 and NM74 in a common fashion via an inverter In80.

In accordance with the above-mentioned configuration according to the present invention, row and column activating operations may not be influenced by any bank selection address during write and read testing operations. That is, the row or column activating operation can be conducted for all banks in a simultaneous manner, thereby enabling a simultaneous read or write test.

That is, in accordance with the present invention, all word lines, in all banks, associated with one row address, can be enabled in every row activating operation. In every column-activating operation, the signal Yi which serves to couple each of bit lines to an associated one of local data bus lines LDB in an enable state thereof is enabled for all banks. Accordingly, the write or read test can be conducted for all banks.

10 In order to prevent data from different banks from fighting with
each other on a data output path, data from each cell passes through
the input/output comparing unit, before it is transmitted to an
associated global read data bus line, so that it is compressed in
5 the input/output comparing unit. Since compressed data is
transmitted to global read data bus lines, there is no data fighting
phenomenon occurring in data output paths.

10 By one write or read cycle, a corresponding write or read
operation is completed for all banks. Accordingly, it is possible
to greatly reduce the entire test time.

15 Now, the operation of the testing apparatus according to the
present invention will be described.

20 When a row active command is inputted to the testing apparatus
in a normal operation mode, it enables a row address strobe signal
which is, in turn, applied to the RAS-generating unit 30. Based on
the row address strobe signal, the RAS-generating unit 30 generates
a row address strobe enabling signal rasatv.

25 On the other hand, when a column active command is inputted is
inputted to the testing apparatus in a normal operation mode, it
enables a column address strobe signal which is, in turn, applied
to the CAS-generating unit 40. Based on the column address strobe
signal, the CAS-generating unit 30 generates a column address strobe
enabling signal casatv.

30 In a test mode in which write and read operations for tests are
to be carried out for all banks, an all-bank test signal tm_abwr is
enabled. This all-bank test signal tm_abwr is applied to respective

gates of the NMOS transistors NM30 and NM40 coupled to respective nodes of the RAS and CAS-generating units 30 and 40, to which a bank selection address signal BA is applied, in a parallel fashion. In this mode, accordingly, row and column activating operations are not
5 influenced by any bank selection address.

In accordance with the above-mentioned configurations of the RAS and CAS-generating units 30 and 40, a chip consisting of N banks can operate such as one bank during write and read tests for all banks.

10 When a write command is inputted, cells included in different banks, but allocated with the same address, are recorded with the same data because each global write data bus line GWDB belongs to all banks.

15 Accordingly, data write is conducted for all banks in a simultaneous manner, thereby enabling a simultaneous write test.

20 When a read operation is subsequently carried out, data from cells included in different banks, but allocated with the same address, are carried on associated bit lines in an amplified state, and then transmitted to associated local data bus lines LDB, respectively, in response to an enabled state of the signal Yi serving to couple each of those bit lines to an associated one of local data bus lines LDB.

25 The data from each local data bus line LDB is then amplified in an associated input/output sense amplifier 50 which, in turn, sends the resultant data to the input/output comparing unit 70.

30 In the test mode, each first transmission gate 61, which serves to couple the output of an associated input/output sense amplifier 50 to an associated global read data bus line GRDB, is closed in

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response to the all-bank test signal tm_abwr, thereby preventing data from the associated input/output sense amplifier 50 from being transmitted to the associated global read data bus line GRDB. On the other hand, each second transmission gate 62, which serves to
5 couple the output of the input/output comparing unit 70 to an associated input/output global read data bus line GRDB, is opened in response to the all-bank test signal tm_abwr, thereby allowing the output from the input/output comparing unit 70 to be transmitted to the associated global read data bus line GRDB. Thus, a data read
10 operation is conducted for all banks in a simultaneous manner.

The input stage of the input/output comparing unit 70 may have various configurations in accordance with the present invention.

15 In accordance with an embodiment of the present invention, respective outputs of input/output sense amplifiers 50 respectively included in different banks, but arranged on the same data path, are coupled to the input of the input/output comparing unit 70.

20 This configuration is illustrated in Fig. 5. In this case, the input/output comparing unit 70 receives, as its input, data from input/output sense amplifiers 50, each being included in one of all banks, carried on the same global data bus line GRDB, as shown in Fig. 5.

25 In this case, it is possible to conduct a data write operation in the test mode, irrespective of the logic level of data to be written, that is, whether data to be written has a low logic level or a high logic level. In a data read operation, the written data can be read
30 in such a fashion that their logic levels are read.

In accordance with another embodiment of the present invention, respective outputs of input/output sense amplifiers 50 included in the same bank are coupled to the input/output comparing unit 70. This configuration is illustrated in Fig. 6.

5

In the case illustrated in Fig. 6, it is necessary to input data having the same logic level in a write operation in the test mode.

In accordance with the multi-bank test system, which is applied to synchronous DRAMs, it is possible to greatly reduce the entire test time, as compared to conventional test systems in which a test is carried out in a special test mode using compressed output data.

As apparent from the above description, the present invention provides a multi-bank testing apparatus for a synchronous DRAM, which allows all banks of the synchronous DRAM to simultaneously carry out their write and read operations in a test mode, thereby being capable of testing the entire bank in order to reduce the test time being likely to increase in accordance with an increased memory integration degree. In order to prevent data from different banks from fighting with each other on a data output path, data from each cell passes through an input/output comparing unit before it is transmitted to an associated global read data bus line, so that it is compressed in the input/output comparing unit.

25

Although the preferred embodiments of the invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.

30

WHAT IS CLAIMED IS:

1. A multi-bank testing apparatus for a synchronous DRAM consisting of a plurality of banks, comprising:

5 a row address strobe generating unit for enabling a word line to transmit data from cells to bit line sense amplifiers in each bank of said synchronous DRAM;

a column address strobe generating unit for generating a signal adapted to enable transistors respectively adapted to couple bit lines carrying data, amplified by said bit line sense amplifiers, to local data bus lines;

10 input/output sense amplifiers for amplifying data on said local data bus lines, respectively;

a transmission gate unit for controlling transmission of data from said input/output sense amplifiers to global read data bus lines; and

15 an input/output comparing unit for compressing data from said input/output sense amplifiers prior to said transmission thereof to said global read data bus lines.

20 2. The multi-bank testing apparatus as claimed in claim 1, wherein said row address strobe generating unit comprises:

a first PMOS transistor and a first NMOS transistor connected in series to each other, said first PMOS and NMOS transistors receiving a row address strobe signal in a common fashion at gates thereof;

a timing controller coupled to a node between said first PMOS and NMOS transistors and adapted to control the period of time for which an output from said row address strobe generating unit;

30 a group of second NMOS transistors coupled in series together and connected in series to said first NMOS transistor, each of said

second NMOS transistors receiving an associated one of bank selection address signals at a gate thereof;

a third NMOS transistor coupled to a node between said first NMOS transistor and said second NMOS transistor group in a fashion parallel to said second NMOS transistor group, said third NMOS transistor receiving, at a gate thereof, an all-bank test signal being enabled when write and read operations in a test mode are to be conducted for all banks.

3. The multi-bank testing apparatus as claimed in claim 1, wherein said column address strobe generating unit comprises:

a first PMOS transistor and a first NMOS transistor connected in series to each other, said first PMOS and NMOS transistors receiving a column address strobe signal in a common fashion at gates thereof;

a timing controller coupled to a node between said first PMOS and NMOS transistors and adapted to control the period of time for which an output from said column address strobe generating unit;

a group of second NMOS transistors coupled in series together and connected in series to said first NMOS transistor, each of said second NMOS transistors receiving an associated one of bank selection address signals at a gate thereof;

a third NMOS transistor coupled to a node between said first NMOS transistor and said second NMOS transistor group in a fashion parallel to said second NMOS transistor group, said third NMOS transistor receiving, at a gate thereof, an all-bank test signal being enabled when write and read operations in a test mode are to be conducted for all banks.

4. The multi-bank testing apparatus as claimed in claim 1, wherein said transmission gate unit comprises:

5 a plurality of first transmission gates each arranged between an output of an associated one of said input/output sense amplifiers and an associated one of said global read data bus lines, each of said first transmission gates being closed in response to an all-bank test signal being enabled when write and read operations in a test mode are to be conducted for all banks, thereby preventing data from said associated input/output sense amplifier from being transmitted to said associated global read data bus line; and

10 a pair of second transmission gates each arranged between an output of said input/output comparing unit and an associated one of said input/output global read data bus lines, each of said second transmission gates being opened by said all-bank test signal, thereby allowing said output from said input/output comparing unit to be transmitted to said associated global read data bus line.

15 5. The multi-bank testing apparatus as claimed in claim 4, wherein:

each of said first transmission gate comprises

20 a first PMOS transistor and a first NMOS transistor coupled in parallel between said associated input/output sense amplifier and a first one of two global read data bus lines respectively associated with input and input-bar signals from said input/output sense amplifier, said first PMOS transistor receiving, at a gate thereof, said all-bank test signal while said first PMOS transistor receiving, at a gate thereof, a signal inverted from said all-bank test signal via an inverter, and

25 a second PMOS transistor and a second NMOS transistor coupled in parallel between said associated input/output sense amplifier and a second one of said associated global read data bus lines, said second PMOS transistor receiving, at a gate thereof, said all-bank test signal while said second NMOS

30

transistor receiving, at a gate thereof, a signal inverted from said all-bank test signal via said inverter; and each of said second transmission gates comprises

5 a third PMOS transistor and a third NMOS transistor coupled in parallel between said input/output comparing unit and said first associated global read data bus line, said third PMOS transistor receiving, at a gate thereof, said signal inverted from said all-bank test signal via said inverter while said third NMOS transistor receiving, at a gate thereof, said all-bank test signal, and

10 a fourth PMOS transistor and a fourth NMOS transistor coupled in parallel between said input/output comparing unit and said second associated global read data bus line, said fourth PMOS transistor receiving, at a gate thereof, said signal
15 inverted from said all-bank test signal via said inverter whereas said fourth NMOS transistor receiving, at a gate thereof, said all-bank test signal.

6. The multi-bank testing apparatus as claimed in claim 1,
20 wherein said input/output comparing unit comprises:

a pair of first PMOS transistors and a pair of first NMOS transistors coupled together in parallel and adapted to receive, at respective gates thereof, a signal inverted by an inverter from an all-bank test signal being enabled when write and read operations
25 in a test mode are to be conducted for all banks;
a plurality of second PMOS transistors coupled in parallel between one of said first PMOS transistors and one of said first NMOS transistors and adapted to receive, at respective gates thereof, input signals;

30 a second NMOS transistor coupled to one of said first NMOS transistors in such a fashion that they have a common source;

a plurality of third PMOS transistors coupled in parallel between the other one of said first PMOS transistors and the other one of said first NMOS transistors and adapted to receive, at respective gates thereof, input-bar signals;

5 a third NMOS transistor connected to other one of said first NMOS transistors in such a fashion that they have a common source;

a first NAND gate adapted to receive said input and input-bar signals;

10 a second NAND gate adapted to receive an output from said first NAND gate at one input thereof, said second NAND gate also receiving said all-bank test signal at the other input thereof; and

15 a third NAND gate adapted to receive an output from said second NAND gate via inverters at one input thereof, said third NAND gate also receiving an output from said second NAND gate via said inverters and then via other inverters, said third NAND gate being coupled at an output thereof to gates of said second and third NMOS transistors in a common fashion via an inverter.

20 7. The multi-bank testing apparatus as claimed in claim 6, wherein said input and input-bar signals are those output from said input/output sense amplifiers transmitted to the same global read data bus line and enabled in response to the same column address.

25 8. The multi-bank testing apparatus as claimed in claim 6, wherein said input and input-bar signals are those output from said input/output sense amplifiers associated with the same bank and enabled in response to the same column address.

ABSTRACT OF THE DISCLOSURE

5 A multi-bank testing apparatus for a synchronous DRAM, which
allows all banks of the synchronous DRAM to simultaneously carry out
their write and read operations in a test mode, thereby being capable
of testing the entire bank in order to reduce the test time being
likely to increase in accordance with an increased memory integration
degree. The multi-bank testing apparatus includes a row address
strobe generating unit for enabling a word line to transmit data from
10 cells to bit line sense amplifiers in each bank of the synchronous
DRAM, a column address strobe generating unit for generating a signal
adapted to enable transistors respectively adapted to couple bit
lines carrying data, amplified by the bit line sense amplifiers, to
local data bus lines, input/output sense amplifiers for amplifying
15 data on the local data bus lines, respectively, a transmission gate
unit for controlling transmission of data from the input/output sense
amplifiers to global read data bus lines, and an input/output
comparing unit for compressing data from the input/output sense
amplifiers prior to the transmission thereof to the global read data
20 bus lines.

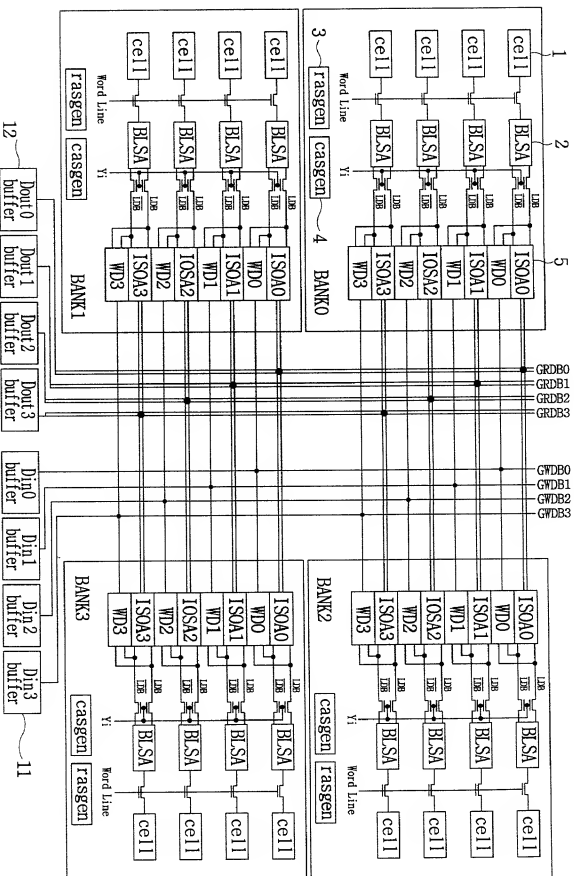


Fig.1(prior art)

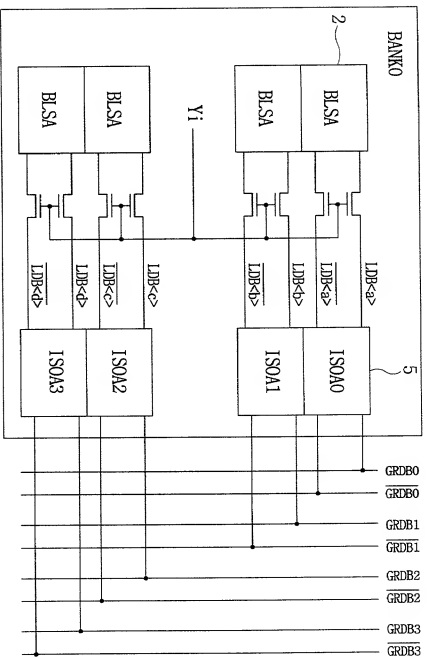


Fig.2(prior art)

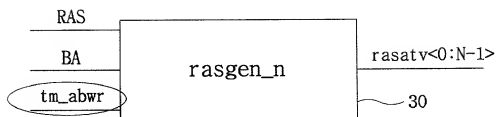


Fig.3A

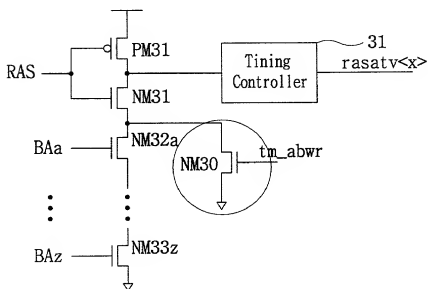


Fig.3B

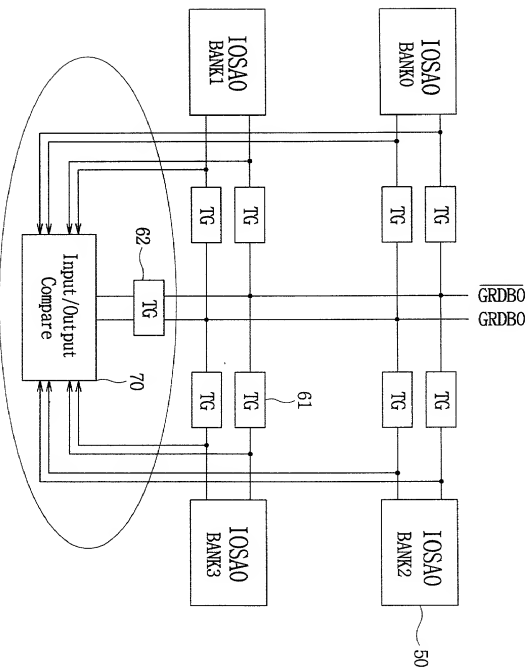
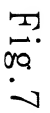


Fig. 5



Fig. 6



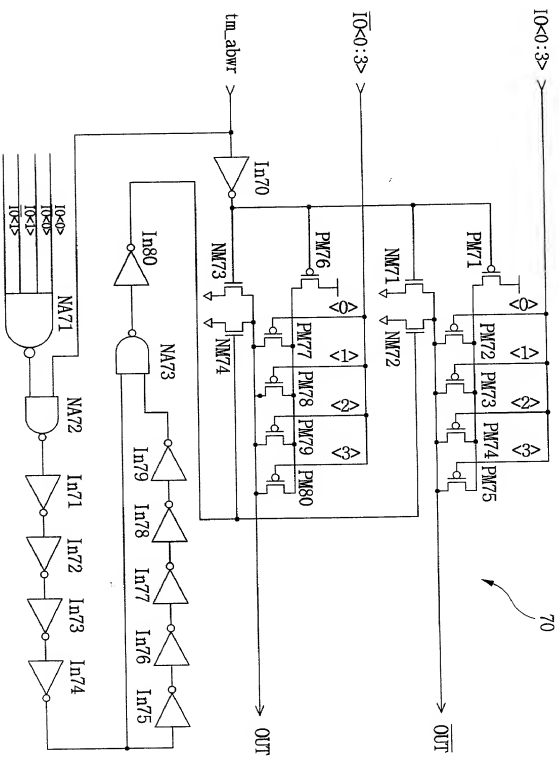


Fig. 8

DECLARATION FOR PATENT APPLICATION

Atty Docket 23900

As the below-named inventors, I/we hereby declare that:

My/Our residences, post office addresses and citizenships are as stated below next to my/our name.

I/we believe I/we are the original inventors of the subject matter which is claimed and for which a patent is sought on the invention entitled:

"A MULTI-BANK TESTING APPARATUS FOR A SYNCHRONOUS DRAM"

the specification of which: (check one)

☒ is attached hereto.

☐ was filed on _____, as Serial No. _____,
and was amended on _____ 19 _____ (if applicable).

I/we hereby state that I/we have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I/we acknowledge the duty to disclose information which is material to the examination of this application in accordance with 37 CFR ☐ 1.56 (a).

I/we hereby claim foreign priority benefits under 35 U.S.C. 119 of any foreign application(s) for patent or inventor's certificate listed below, and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Applications:

<u>98-18885</u> (Application No.)	<u>Korea</u> (Country)	<u>25/05/1998</u> (Day/Month/Year Filed)	Priority Claimed <input checked="" type="checkbox"/> <input type="checkbox"/> Yes No
<u> </u> (Application No.)	<u> </u> (Country)	<u> / / </u> (Day/Month/Year Filed)	<input type="checkbox"/> <input type="checkbox"/> Yes No
<u> </u> (Application No.)	<u> </u> (Country)	<u> / / </u> (Day/Month/Year Filed)	<input type="checkbox"/> <input type="checkbox"/> Yes No

I/we hereby appoint Gary M. Nath, Reg. No. 26,865; Irvin A. Lavine, Reg. No. 16,838; Suet M. Chong, Reg. No. 38,104; and Anthony D. Miller, Reg. No. 34,394 as my attorneys to prosecute this application and transact all business in the U.S. Patent and Trademark Office connected therewith.

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NATH & ASSOCIATES
6th Floor
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Washington, D.C. 20005 U.S.A.

I/we hereby claim the benefit under 35 U.S.C. ☐ 120 of any United States Application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by 35 U.S.C. ☐ 112, first paragraph, I/we acknowledge the duty to disclose material information as defined in 37 CFR ☐ 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

(U.S. Application Serial No.) (U.S. Filing Date) (Status--patented, pending, abandoned)

(U.S. Application Serial No.) (U.S. Filing Date) (Status--patented, pending, abandoned)

I/we hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. ☐ 1001 and that such willful false statements may jeopardize the validity of the application of any patent issued thereon.

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Inventors's Signature *Chang Ho Do* Date March 11, 1989

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Full name of second inventor: _____

Inventors's Signature _____ Date _____

Residence: _____

Citizenship: _____

Post Office Address: _____

Full name of third inventor: _____

Inventors's Signature _____ Date _____

Residence: _____

Citizenship: _____

Post Office Address: _____